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Document Identifier: DSP0239

Date: 2021-02-18

Version: 1.7.1

Management Component Transport Protocol (MCTP) IDs and Codes

7 Supersedes: 1.7.0

Document Class: Normative 8

9 **Document Status: Published**

10 Document Language: en-US

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62	Foreword				
63 64	The Management Component Transport Protocol (MCTP) IDs and Codes (DSP0239) was prepared by the PMCI Working Group.				
65 66	DMTF is a not-for-profit association of industry members dedicated to promoting enterprise and systems management and interoperability.				
67	Acknowledgments				
68	The DMTF acknowledges the following individuals for their contributions to this document:				
69	Editors:				
70	Hemal Shah – Broadcom Inc.				
71	Tom Slaight – Intel Corporation				
72	Philip Chidester – Dell Inc.				
73	Edward Newman – Hewlett Packard Enterprise				
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75	Alan Berenbaum – SMSC				
76	Patrick Caporale – Lenovo				
77	Kelly Couch – Intel Corporation				
78	Yuval Itkin – NVIDIA Corporation				
79	Janusz Jurski – Intel Corporation				
80	Ed Klodnicki – IBM				
81	Patrick Kutch – Intel Corporation				
82	Eliel Louzoun – Intel Corporation				
83	Zvika Perry – Cavium				
84	Bob Stevens – Dell Technologies				
85	Supreeth Venkatesh – Advanced Micro Devices				

DSP0239

Management Component Transport Protocol (MCTP) IDs and Codes

86	Introduction			
87 88	This document presents a collection of IDs and codes that are used across the Management Componen Transport Protocol (MCTP) and transport binding specifications.			
89	The MCTP defines a communication model intended to facilitate communication between:			
90	 Management controllers and other management controllers 			
91	Management controllers and management devices			
92 93	The communication model includes a message format, transport description, message exchange patterns, and configuration and initialization messages.			
94 95 96 97 98	The MCTP Base Protocol Specification (DSP0236) describes the protocol and commands used for communication within and initialization of an MCTP network. Associated with the Base Protocol Specification are transport binding specifications that define how the MCTP base protocol and MCTP control commands are implemented on a particular physical transport type and medium.			

Scope

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Management Component Transport Protocol (MCTP) IDs and Codes

103 104 105 106 107	The Management Component Transport Protocol (MCTP) IDs and Codes document provides a consolidated list of major IDs and codes used across the MCTP protocol and transport binding specifications. Only IDs and codes that are required by a particular specification should be included in that specification. IDs and codes values for other specifications should not be repeated for reference. Instead, a reference to this specification should be provided.
108 109	The following is an overview of the different sets of codes and identifiers (enumeration values) that are specified in this document:
110	MCTP message type codes
111	Collection of the message type codes used for MCTP messages
112	MCTP physical medium identifiers
113	Collection of identifiers for the different types of physical media that have been defined
114	MCTP physical transport binding identifiers
115 116	Collection of identifiers for the specifications that define the operation, formatting, addressing, and encapsulation of MCTP packets over different physical media
117	MCTP host interface type identifiers
118 119	Collection of identifiers for the different physical interfaces used to transfer MCTP packets between the host and the management controller
120	2 Normative references
121 122 123 124	The following referenced documents are indispensable for the application of this document. For dated or versioned references, only the edition cited (including any corrigenda or DMTF update versions) applies For references without a date or version, the latest published edition of the referenced document (including any corrigenda or DMTF update versions) applies.
125 126 127	DMTF specifications are available at http://www.dmtf.org/standards/published_documents . Unless otherwise specified, values defined in this document apply to all published DMTF Standard versions of the particular referenced DMTF specification.
128	DMTF DSP0134, SMBIOS Reference Specification
129	DMTF DSP0222, Network Controller Sideband Interface (NC-SI) Specification
130	DMTF DSP0235, NVMe (NVM Express) Management Messages over MCTP Binding Specification
131	DMTF DSP0236, Management Component Transport Protocol (MCTP) Base Specification
132 133	DMTF DSP0237, Management Component Transport Protocol (MCTP) SMBusI ² C Transporting Binding Specification
134 135	DMTF DSP0238, Management Component Transport Protocol (MCTP) PCle VDM Transport Binding Specification
136	DMTF DSP0241, PLDM Over MCTP Binding Specification

- 137 DMTF DSP0253, MCTP Serial Transport Binding Specification
- 138 DMTF DSP0254, MCTP KCS Transport Binding Specification
- 139 DMTF DSP0261, NC-SI Over MCTP Binding Specification
- 140 DMTF DSP0275, Security Protocol and Data Model (SPDM) over MCTP Binding Specification
- 141 DMTF DSP0276, Secured Messages using SPDM over MCTP Binding Specification
- 142 ISO/IEC Directives, Part 2, Rules for the structure and drafting of International Standards,
- 143 http://isotc.iso.org/livelink/livelink?func=ll&objId=4230456&objAction=browse&sort=subtype
- PCI-SIG, PCI Express Base Specification 1.1, PCIeV1.1, March 28, 2005, http://pcisig.com/specifications
- PCI-SIG, PCI Express Base Specification 2.0, PCIeV2.1, March 4, 2009, http://pcisig.com/specifications
- PCI-SIG, PCI Express Base Specification 3.0, PCIeV3.0, November 10, 2010,
- 147 http://pcisig.com/specifications
- PCI-SIG, PCI Express Base Specification 4.0, PCIeV4.0, October 5, 2017, http://pcisig.com/specifications
- PCI-SIG, PCI Express Base Specification 5.0, PCIeV5.0, May 28, 2019, http://pcisig.com/specifications
- 150 NXP Semiconductors, I²C-bus specification and user manual, Rev. 6, 4 April 2014
- 151 http://www.nxp.com/documents/user_manual/UM10204.pdf
- 152 SMBus, System Management Bus (SMBus) Specification v2.0, SMBus, 2000,
- 153 http://www.smbus.org/specs/smbus20.pdf
- 154 SMBus, System Management Bus (SMBus) Specification v3.0, SMBus, December 20, 2014,
- http://www.smbus.org/specs/SMBus 3 0 20141220.pdf
- 156 MIPI Alliance Specification for I3C® (Improved Inter Integrated Circuit), version 1.0, MIPI Alliance, Inc.,
- 157 23 December 2016 (Adopted 31 December 2016), https://www.mipi.org/specifications/i3c-sensor-
- 158 specification.
- 159 MIPI Alliance Specification for I3C BasicSM (Improved Inter Integrated Circuit Basic), version 1.0, MIPI
- Alliance, Inc., 19 July 2018 (Adopted 8 October 2018), http://resources.mipi.org/mipi-i3c-basic-v1-
- 161 download.
- 162 CXL™ 1.1 Specification and the CXL 1.1 Errata, https://www.computeexpresslink.org/download-the-
- 163 specification

164 3 Terms and definitions

Refer to DSP0236 for terms and definitions that are used in the MCTP specifications.

166 4 Symbols and abbreviated terms

Refer to <u>DSP0236</u> for symbols and abbreviated terms that are used in the MCTP specifications.

168 **5 Conventions**

The conventions described in the following clauses apply to this specification.

170 5.1 Reserved and unassigned values

- 171 Unless otherwise specified, any reserved, unspecified, or unassigned values in enumerations or other
- 172 numeric ranges are reserved for future definition by the DMTF.
- 173 Unless otherwise specified, numeric or bit fields that are designated as reserved shall be written as 0
- 174 (zero) and ignored when read.

175 **5.2 Byte ordering**

- 176 Unless otherwise specified, byte ordering of multi-byte numeric fields or bit fields is "Big Endian" (that is,
- the lower byte offset holds the most significant byte, and higher offsets hold lesser significant bytes).

6 MCTP Message Type codes

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- Table 1 defines the values for the Message Type field for different message types transported through MCTP.
- NOTE A device that supports a given message type may not support that message type equally across all busses that connect to the device.

Table 1 – MCTP Message Types

Message Type	Message Type Code	Description
MCTP Control	0x00	Messages used to support initialization and configuration of MCTP communication within an MCTP network, as specified in DSP0236
Platform Level Data Model (PLDM)	0x01	Messages used to convey Platform Level Data Model (PLDM) traffic over MCTP, as specified in DSP0241.
NC-SI over MCTP	0x02	Messages used to convey NC-SI Control traffic over MCTP, as specified in DSP0261.
Ethernet over MCTP	0x03	Messages used to convey Ethernet traffic over MCTP. See DSP0261. This message type can also be used separately by other specifications.
NVM Express Management Messages over MCTP	0x04	Messages used to convey NVM Express (NVMe) Management Messages over MCTP, as specified in DSP0235.
SPDM over MCTP	0x05	Messages used to convey Security Protocol and Data Model Specification (SPDM) traffic over MCTP, as specified in DSP0275.
Secured Messages	0x06	Messages used to convey Secured Messages using SPDM over MCTP Binding Specification traffic, as specified in DSP0276.
Vendor Defined – PCI	0×7E	Message type used to support VDMs where the vendor is identifed using a PCI-based vendor ID. The specification of the initial Message Header bytes for this message type is provided within this specification. The specification of the format of this message is given in DSP0236 . Otherwise, the message body content is specified by the vendor, company, or organization identified by the given vendor ID.
Vendor Defined – IANA	0x7F	Message type used to support VDMs where the vendor is identifed using an IANA-based vendor ID. This format uses an "Enterprise Number" that is assigned and maintained by the Internet Assigned Numbers Authority (IANA), www.iana.org , as the means of identifying a particular vendor, company, or organization. The specification of the format of this message is given in DSP0236 . Otherwise, the message body content is specified by the vendor, company, or organization identified by the given vendor ID.
Reserved	all other	Reserved

7 MCTP physical medium identifiers

- Table 2 defines a set of numbers that correspond to different media types that can be used with MCTP.
- 186 The identifier is primarily used to identify which physical addressing format is used for MCTP packets on
- 187 the bus.
- 188 NOTE PCIe revision numbers are intended to indicate specification compatibility, not bit transfer rate or
- 189 throughput.
- 190

Table 2 - MCTP physical medium identifiers

0x00 Unspecified 0x01 SMBus 2.0 100 kHz compatible 0x02 SMBus 2.0 + I²C 100 kHz compatible 0x03 I²C 100 kHz compatible (Standard-mode) 0x04 SMBus 3.0 or I²C 400 kHz compatible (Fast-mode) 0x05 SMBus 3.0 or I²C 1 MHz compatible (Fast-mode Plus) 0x06 I²C 3.4 MHz compatible (High-speed mode) 0x07 Reserved 0x08 PCle revision 1.1 compatible 0x09 PCle revision 2.0 compatible 0x0A PCle revision 2.1 compatible 0x0B PCle revision 3.x compatible 0x0C PCle revision 4.x compatible 0x0D PCle revision 5.x compatible 0x0E Reserved 0x0F PCI compatible (PCI 1.0,2.0,2.1,2.2,2.3,3.0,PCI-X 1.0, PCI-X 2.0) 0x10 USB 1.1 compatible 0x11 USB 2.0 compatible 0x12 USB 3.0 compatible 0x13:0x17 Reserved 0x13:0x17 Reserved 0x20 KCS¹ / Legacy (Fixed Address Decoding) 0x21 KCS¹ / PCI (Base Class 0xC0 Subclass 0x01) 0x22	Physical Media Identifier	Description
0x02 SMBus 2.0 + IPC 100 kHz compatible 0x03 IPC 100 kHz compatible (Standard-mode) 0x04 SMBus 3.0 or IPC 400 kHz compatible (Fast-mode) 0x05 SMBus 3.0 or IPC 1 MHz compatible (Fast-mode Plus) 0x06 IPC 3.4 MHz compatible (High-speed mode) 0x07 Reserved 0x08 PCIe revision 1.1 compatible 0x09 PCIe revision 2.0 compatible 0x00 PCIe revision 2.1 compatible 0x00 PCIe revision 3.x compatible 0x00 PCIe revision 4.x compatible 0x00 PCIe revision 5.x compatible 0x00 PCI compatible (PCI 1.0,2.0,2.1,2.2,2.3,3.0,PCI-X 1.0, PCI-X 2.0) 0x10 USB 1.1 compatible 0x11 USB 2.0 compatible 0x12 USB 3.0 compatible 0x13:0x17 Reserved 0x18 NC-SI over RBT (A physical interface based on RMII as defined in DSP0222) 0x19:0x1F Reserved 0x20 KCSI / Legacy (Fixed Address Decoding) 0x21 KCSI / PCI (Base Class 0xC0 Subclass 0x01) 0x22 Serial Host² / PCI (Base Class 0xO7 Subclass 0x00)	0x00	Unspecified
0x03 I²C 100 kHz compatible (Standard-mode) 0x04 SMBus 3.0 or I²C 400 kHz compatible (Fast-mode) 0x05 SMBus 3.0 or I²C 1 MHz compatible (Fast-mode) 0x06 I²C 3.4 MHz compatible (High-speed mode) 0x07 Reserved 0x08 PCIe revision 1.1 compatible 0x09 PCIe revision 2.0 compatible 0x0A PCIe revision 3.x compatible 0x0B PCIe revision 4.x compatible 0x0C PCIe revision 5.x compatible 0x0D PCIe revision 5.x compatible 0x0E Reserved 0x0F PCI compatible (PCI 1.0,2.0,2.1,2.2,2.3,3.0,PCI-X 1.0, PCI-X 2.0) 0x10 USB 1.1 compatible 0x11 USB 2.0 compatible 0x12 USB 3.0 compatible 0x12 USB 3.0 compatible 0x13:0x17 Reserved 0x20 KCS1 / Legacy (Fixed Address Decoding) 0x21 KCS1 / Legacy (Fixed Address Decoding) 0x22 Serial Host² / Legacy (Fixed Address Decoding) 0x23 Serial Host² / PCI (Base Class 0x07 Subclass 0x00) 0x30 I3C Basic compatible	0x01	SMBus 2.0 100 kHz compatible
0x04 SMBus 3.0 or I²C 400 kHz compatible (Fast-mode) 0x05 SMBus 3.0 or I²C 1 MHz compatible (Fast-mode Plus) 0x06 I²C 3.4 MHz compatible (High-speed mode) 0x07 Reserved 0x08 PCIe revision 1.1 compatible 0x09 PCIe revision 2.0 compatible 0x0A PCIe revision 2.1 compatible 0x0B PCIe revision 3.x compatible 0x0C PCIe revision 4.x compatible 0x0D PCIe revision 5.x compatible 0x0E Reserved 0x0F PCI compatible (PCI 1.0,2.0,2.1,2.2,2.3,3.0,PCI-X 1.0, PCI-X 2.0) 0x10 USB 1.1 compatible 0x11 USB 2.0 compatible 0x12 USB 3.0 compatible 0x12 USB 3.0 compatible 0x13:0x17 Reserved 0x19:0x1F Reserved 0x20 KCS¹ / Legacy (Fixed Address Decoding) 0x21 KCS¹ / PCI (Base Class 0xC0 Subclass 0x01) 0x22 Serial Host² / PCI (Base Class 0xC7 Subclass 0x00) 0x23 Serial Host² / PCI (Base Class 0xC7 Subclass 0x00) 0x24 Asynchronous Serial³ (Between MCs and I	0x02	SMBus 2.0 + I ² C 100 kHz compatible
0x05 SMBus 3.0 or I²C 1 MHz compatible (Fast-mode Plus) 0x06 I²C 3.4 MHz compatible (High-speed mode) 0x07 Reserved 0x08 PCIe revision 1.1 compatible 0x09 PCIe revision 2.0 compatible 0x0A PCIe revision 2.1 compatible 0x0B PCIe revision 3.x compatible 0x0C PCIe revision 4.x compatible 0x0D PCIe revision 5.x compatible 0x0E Reserved 0x0F PCI compatible (PCI 1.0,2.0,2.1,2.2,2.3,3.0,PCI-X 1.0, PCI-X 2.0) 0x10 USB 1.1 compatible 0x11 USB 2.0 compatible 0x12 USB 3.0 compatible 0x13:0x17 Reserved 0x18 NC-SI over RBT (A physical interface based on RMII as defined in DSP0222) 0x19:0x1F Reserved 0x20 KCS¹ / Legacy (Fixed Address Decoding) 0x21 KCS¹ / PCI (Base Class 0xC0 Subclass 0x01) 0x22 Serial Host² / Legacy (Fixed Address Decoding) 0x23 Serial Host² / PCI (Base Class 0xO7 Subclass 0x00) 0x24 Asynchronous Serial³ (Between MCs and IMDs) 0x30	0x03	I ² C 100 kHz compatible (Standard-mode)
0x06 IPC 3.4 MHz compatible (High-speed mode) 0x07 Reserved 0x08 PCIe revision 1.1 compatible 0x09 PCIe revision 2.0 compatible 0x0A PCIe revision 2.1 compatible 0x0B PCIe revision 3.x compatible 0x0C PCIe revision 4.x compatible 0x0D PCIe revision 5.x compatible 0x0E Reserved 0x0F PCI compatible (PCI 1.0,2.0,2.1,2.2,2.3,3.0,PCI-X 1.0, PCI-X 2.0) 0x10 USB 1.1 compatible 0x11 USB 2.0 compatible 0x12 USB 3.0 compatible 0x13:0x17 Reserved 0x18 NC-SI over RBT (A physical interface based on RMII as defined in DSP0222) 0x19:0x1F Reserved 0x20 KCS1 / Legacy (Fixed Address Decoding) 0x21 KCS1 / PCI (Base Class 0x00 Subclass 0x01) 0x22 Serial Host² / Legacy (Fixed Address Decoding) 0x23 Serial Host² / Legacy (Fixed Address Decoding) 0x24 Asynchronous Serial³ (Between MCs and IMDs) 0x30 I3C Basic compatible 0x40 CXL 1.x <td>0x04</td> <td>SMBus 3.0 or I²C 400 kHz compatible (Fast-mode)</td>	0x04	SMBus 3.0 or I ² C 400 kHz compatible (Fast-mode)
0x07 Reserved 0x08 PCIe revision 1.1 compatible 0x09 PCIe revision 2.0 compatible 0x0A PCIe revision 2.1 compatible 0x0B PCIe revision 3.x compatible 0x0C PCIe revision 4.x compatible 0x0D PCIe revision 5.x compatible 0x0E Reserved 0x0F PCI compatible (PCI 1.0,2.0,2.1,2.2,2.3,3.0,PCI-X 1.0, PCI-X 2.0) 0x10 USB 1.1 compatible 0x11 USB 2.0 compatible 0x12 USB 3.0 compatible 0x12 USB 3.0 compatible 0x12 USB 3.0 compatible 0x13:0x17 Reserved 0x18 NC-SI over RBT (A physical interface based on RMII as defined in DSP0222) 0x19:0x1F Reserved 0x20 KCS¹ / Legacy (Fixed Address Decoding) 0x21 KCS¹ / PCI (Base Class 0xC0 Subclass 0x01) 0x22 Serial Host² / PCI (Base Class 0xO7 Subclass 0x00) 0x24 Asynchronous Serial³ (Between MCs and IMDs) 0x30 I3C Basic compatible 0x40 CXL 1.x	0x05	SMBus 3.0 or I ² C 1 MHz compatible (Fast-mode Plus)
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0x30 I3C Basic compatible 0x31:0x3F Reserved 0x40 CXL 1.x	0x23	Serial Host ² / PCI (Base Class 0x07 Subclass 0x00)
0x31:0x3F Reserved 0x40 CXL 1.x	0x24	Asynchronous Serial ³ (Between MCs and IMDs)
0x40 CXL 1.x	0x30	I3C Basic compatible
	0x31:0x3F	Reserved
0x41:0xFF Reserved	0x40	CXL 1.x
	0x41:0xFF	Reserved

^{1.} Keyboard Controller Style Interface – refer to <u>DSP0254</u>.

^{2.} Serial Host refers to a register based UART interface.

^{3.} Asynchronous Serial refers to an 8-bit asynchronous bi-directional serial transmission media where characters are transmitted independently (i.e., each frame carries 8-bits of data).

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8 MCTP physical transport binding identifiers

Table 3 defines as set of numbers that correspond to different media types that can be used with MCTP.
The identifier indicates which physical addressing format is used for MCTP packets on the bus.

Table 3 - MCTP physical transport binding identifiers

MCTP Physical Transport Binding Identifier	Description
0x00	Reserved
0x01	MCTP over SMBus (DSP0237)
0x02	MCTP over PCIe VDM (<u>DSP0238</u>)
0x03	Reserved for MCTP over USB
0x04	MCTP over KCS (<u>DSP0254</u>)
0x05	MCTP over Serial (<u>DSP0253</u>)
0xff	Vendor defined NOTE A vendor-defined transport binding must meet the requirements in DSP0236 (in particular, when being bridged to or from standard MCTP transport binding and media combinations).
All other	Reserved

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9 MCTP host interface type identifiers

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The SMBIOS specification (DSP0134) reserves a range of host interface type identifiers 0x00 through 0x3F for use by this specification. Table 4 defines a set of numbers that correspond to different MCTP host interface types that can be used with MCTP. The identifier indicates which physical interface to transfer MCTP packets between the host and the management controller.

Table 4 - MCTP host interface type identifiers

MCTP Host Interface Type Identifier	Description
0x00	Reserved
0x01	Reserved
0x02	KCS: Keyboard Controller Style – refer to <u>Intelligent Platform</u> <u>Management Interface Specification</u> Section 9 Keyboard Controller Style (KCS) Interface
0x03	8250 UART Register Compatible
0x04	16450 UART Register Compatible
0x05	16550/16550A UART Register Compatible
0x06	16650/16650A UART Register Compatible
0x07	16750/16750A UART Register Compatible
0x08	16850/16850A UART Register Compatible
0x09:0x3F	Reserved
all other	Assigned by the SMBIOS specification (DSP0134)

10 Host interface protocol identifiers

In earlier versions of this specification, this section contained a table of host interface protocol identifiers. That table has been moved to the description of the Type 42 record of the SMBIOS specification (DSP0134) with a version greater than 3.1.0.

209			ANNEX A
210			(informative)
211			Notation and conventions
212	Notatio	ons	
213	Example	es of notat	tions used in this document are as follows:
214 215 216	•	2:N	In field descriptions, this will typically be used to represent a range of byte offsets starting from byte two and continuing to and including byte N. The lowest offset is on the left, the highest is on the right.
217 218	•	(6)	Parentheses around a single number can be used in message field descriptions to indicate a byte field that may be present or absent.
219 220	•	(3:6)	Parentheses around a field consisting of a range of bytes indicates the entire range may be present or absent. The lowest offset is on the left, the highest is on the right.
221 222 223	•	<u>PCle</u>	Underlined, blue text is typically used to indicate a reference to a document or specification called out in the "Normative References" section or to items hyperlinked within the document.
224	•	rsvd	Abbreviation for "reserved." Case insensitive.
225 226	•	[4]	Square brackets around a number are typically used to indicate a bit offset. Bit offsets are given as zero-based values (that is, the least significant bit [LSb] offset = 0).
227 228	•	[7:5]	A range of bit offsets. The most significant bit is on the left, the least significant bit is on the right.
229 230	•	1b	The lower case "b" following a number consisting of $0s$ and $1s$ is used to indicate the number is being given in binary format.
231	•	0x12A	A leading " $0x$ " is used to indicate a number given in hexadecimal format.
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ANNEX B (informative) Change log

Version	Date	Description
1.0.0	2009-07-28	
1.1.0	2009-11-03	Added Host Interface Type Identifiers. Added Host Interface Protocol Identifiers. Added reference to NC-SI and added clarification on physical medium identifiers.
1.2.0	2012-06-04	Added Ethernet over MCTP message type. Clarified the description of NC-SI over MCTP and PLDM over MCTP. Added I2C fast plus and high-speed physical medium identifiers. Clarified RMII/NC-SI physical medium identifier description. Fixed references.
1.3.0	2015-03-06	Added message type NVMe (NVM Express) Management Messages over MCTP. Updated references.
1.4.0	2017-01-11	Limited host interface type identifiers to the range 0x00:0x3F. Moved the host interface protocol identifier table to the SMBIOS specification. Updated references.
1.5.0	2017-11-16	Updated contributors and references. Added support for SMBus 3.0 and PCle Gen 4.
1.6.0	2019-06-04	Added an MCTP Message Type for SPDM. Added an MCTP physical medium identifiers for PCIe revision 5.0, and I3C.
1.7.0	2020-05-05	Added an MCTP Message Type for MCTP Security using SPDM. Added an MCTP physical medium identifiers for CXL.
1.7.1	2021-01-19	Update the contributor list. Correct the I3C entries in the MCTP physical medium identifiers table.

DSP0239

Management Component Transport Protocol (MCTP) IDs and Codes

236	Bibliography
237 238	RMII Consortium, Reduced Media Independent Interface (RMII) Specification v1.2, RMII, March 20, 1988 http://ebook.pldworld.com/_eBook/-Telecommunications,Networks-/TCPIP/RMII/rmii_rev12.pdf
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